In the Specification

Please replace the paragraph starting on page 5, line 23 with:

It should be understood by those skilled in the related arts that all circuitry subsequent to the analog-to-digital converters, i.e., circuits 20_1, 20_2,..., 20_B and 22 typically would be digital and may be implemented by a digital signal processor (DSP), a processor, a ~~microprocessor an~~ microprocessor, an application specific integrated circuit, a finite state machine, a programmed general purpose computer or any other equivalent (hereinafter collectively "DSP"). In fact, because of the large amount of processing needed to generate the path estimates and path estimate errors from the beams, the flat fading multipath and multiuser estimation and the minimum variance selection typically is performed by a bank of DSPs.

A1

Please replace the paragraph on page 23, lines 10-13 with:

Objective Functions: Compute the chip-rate beamforming vector sequences ~~$\hat{F}_{G-1} \stackrel{\Delta}{=} (\hat{f}_o, \hat{f}_2, \ldots, \hat{f}_{G-1})$~~ $\hat{F}_{G-1} \stackrel{\Delta}{=} (\hat{f}_o, \hat{f}_1, \ldots, \hat{f}_{G-1})$ and $\hat{\hat{F}}_{G-1} \stackrel{\Delta}{=} (\hat{\hat{f}}_o, \hat{\hat{f}}_2, \ldots, \hat{\hat{f}}_{G-1})$ which respectively maximize the terminal cost function $h_{G-1} = E\{(\chi_{G-1} - \chi_{G-1|G-1})^H J(\chi_{G-1} - \chi_{G-1|G-1})\}$ as follows

A2

Please replace the equation on page 24, line 5 with

2. ~~$\hat{F}_{G-1} = \arg\max_{F_{g-1}} Tr\{JP_{G-1G-1}(F_{G-1})\}$~~ $\hat{F}_{G-1} = \arg\max_{F_{G-1}} Tr\{JP_{G-1G-1}(F_{G-1})\}$

A3

On page 24, line 5, please replace equation 48 with

~~$$P_{k|k}(F_k) = P_{k|k-1}(F_{k-1})\left[I - f_k A^H(\phi) S^{-1}_{k|k-1}(F_k) f_k^H(\phi) P_{k|k-1}(F_{k-1})\right]$$~~

$$P_{k|k}(F_k) = P_{k|k-1}(F_{k-1})\left|I - f_k A^H(\phi) S^H_{k|k-1}(F_k) f_k^H A(\phi) P_{k|k-1}(F_{k-1})\right|$$